UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,919,749 B2
DATED : July 19, 2005
INVENTOR(S) : Alon et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 13,
Line 65, please change to read -- the second storage device; and --.

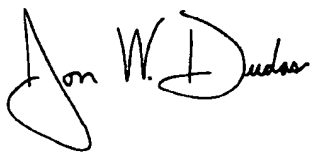
Column 14,
Line 64, please change to read -- a second input terminal for receiving a second signal; --.

Column 15,
Line 24, please change to read -- the second storage device; and; --.
Lines 30-31, please change to read -- multiplexor, the fourth multiplexor, the fifth multiplexor, and the sixth multiplexor. --.

Column 16,
Line 7, please change to read -- 17. A circuit comprising:
a first delay line having a first set of output taps and --.
Line 39, please change to read -- the second storage device; and --.

Signed and Sealed this

Eleventh Day of October, 2005



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Director of the United States Patent and Trademark Office